REMARKS

In response to the Office Action mailed May 17, 2004, Applicants amend their application and request reconsideration. In this Amendment, no claims are cancelled or added so that claims 1-7 remain pending. Claim 6 was indicated as allowable and therefore does not require further comment although its ultimate parent claim 1 is amended.

In this Amendment the claims have been amended for clarity. As described in the patent application, the invention pertains to circuit that protects a power semiconductor device, such as an insulated gate bipolar transistor (IGBT), from damage due to a short circuit. The invention is particularly directed to preventing damage to such a power semiconductor device upon the application of a turn-on or turn-off instruction to the device. As explained in the patent application, when a short circuit occurs during turn-on or turn-off of the device, a very large current can flow through the device. If the large current flows for too long, the device is permanently damaged or destroyed.

As described in claim 1, the drive circuit includes a control means that controls switching of the device in response to a turn-on or turn-off instruction applied to the drive circuit. Then, during the turning on of the power semiconductor device, the value of an electrical variable that is applied to a control terminal of the power semiconductor device is monitored. The monitoring occurs during a time period when the control means receives the turn-on instruction. Then, a determination is made as to whether a short circuit has occurred by monitoring the value of the electrical variable. That time interval extends until before an electrical variable related to a control terminal of the power semiconductor device reaches a threshold voltage if there is no abnormality, e.g., short circuit, across the power semiconductor device or in a load switched by the power semiconductor device. As explained in the patent application, during this time period, if there is an abnormality, e.g., a short circuit, this electrical variable at the control terminal of the power semiconductor device reaches or exceeds or fails to reach a threshold value, e.g., a predetermined voltage value. When that value is reached, or not reached if total charge flowing into the gate is monitored, during the time period, then it is apparent that an abnormality has occurred and appropriate action is to be taken. As explained in the patent application and mentioned in claims 5 and 6, one reaction that is taken in the event of the detection of an abnormality is to turn off the power semiconductor device.

In this Amendment the monitoring of the electrical variable at the control terminal of the power semiconductor device is clarified. In the illustrated embodiments, the power

semiconductor device is an IGBT so the control terminal is the base of the IGBT. The control terminal could be the gate of a transistor.

Claim 4 was rejected as indefinite and the Examiner requested an explanation of the relationship between claim 4 and Figure 7. However, claim 4 relates to the description pertaining to Figure 11, not the description pertaining to Figure 7. Comparison of claim 4 to Figure 11 shows that there is no indefiniteness in claim 4. It can be seen that the detection time period of Figure 11 corresponds to the transition time period of claim 4. The gate voltage, under normal conditions, i.e., the electrical variable at the control terminal, does not reach the reference value shown in the top curve of Figure 11 before the expiration of that time period. In the second graph from the top in Figure 11, it can be seen that the gate voltage reaches the reference value during the transition time period, indicating an abnormality.

With the exception of claim 6, all of the examined claims were rejected as anticipated by Kiraly (U.S. Patent 5,467,242). This rejection is respectfully traversed.

Kiraly has essentially the same objective as the present invention, namely the protection of an IGBT from the effects of short circuiting. This protection is provided in Kiraly by monitoring the voltage at terminal 55, i.e., at the collector of the transistor 50. There is no monitoring of the voltage or another electrical variable at the base or gate of the transistor 50. The Examiner directed attention to Figure 2 of Kiraly and the first pertinent passage in Kiraly, which appears in column 4, lines 27-31. That paragraph explains that the timer 20 shown in Figure 2 of Kiraly protects the power semiconductor device during turn-on, preventing false triggering of the protection circuit which would otherwise turn off the IGBT in order to avoid damage to that switching transistor. However, the description in column 4 of Kiraly is not the complete description in that patent as to what is disclosed. That description must be considered in connection with Figures 5 and 6, and particularly Figure 6, and the description that pertains to that figure. As explained at columns 5 and 6 of Kiraly, the timer 20 essentially disables the comparator 10 so that it is impossible to monitor, during an initial turn-on time period, the voltage across the IGBT. In other words, in order to avoid a false indication of a failure due to a residual high collector to emitter voltage, the protective circuitry of Kiraly is simply taken out of service. The absence of monitoring during the initial turn-on period is essential in Kiraly since Kiraly monitors that collector-to-emitter voltage, not a voltage at the control terminal. This approach is opposite the monitoring function of the drive circuit described and claimed in the present patent application. This difference alone shows that the rejection for anticipation is incorrect.

This operation of the Kiraly circuit is made clear in the passage beginning in column 6, lines 7-29. Referring to Figure 6, a blanking circuit 130 is described as disabling the protective circuit for a fixed time period, namely 500 nanoseconds. This blanking circuit corresponds to the timer 20 of Figure 2 of Kiraly. As described in column 6, the blanking circuit 130 includes an input 132 that delays the protection provided by the circuit, not only upon the receipt of a turn-on instruction, but also in the event of an apparent error so that minor changes in current flow or voltage do not automatically result in opening of the IGBT switch. As discussed in column 6, lines 24-29 of Kiraly, the logic control input 132 removes the disable signal applied to the driver 60, i.e., the comparator 10 in Figure 2 of Kiraly when the input voltage is zero.

To summarize, what is described in Kiraly with respect to Figures 2, 5, and 6, is that a comparator 10, triggering a timer 30 concerned with turning off the IGBT, is disabled after a turn-on instruction is applied to the driver 60. The disabling occurs through a timer 20 for a fixed length blanking period. After the expiration of the blanking period, when the IGBT is assumed to have turned on, operation is monitored for potential turning off of the IGBT through the comparator 10 and the timer 30. This arrangement is, at best, the opposite of the invention as defined the claims now presented.

As described, in the invention, the period of monitoring (not disabling) the electrical variable at the control terminal of the power semiconductor device, according to claim 1, occurs during a period when a turn-on signal is received. The monitoring continues until a time just before the time the electrical variable at the control terminal of the power semiconductor device would reach a threshold voltage if there is no abnormality, e.g., a short circuit. In Kiraly, through the disabling function of the timer 20, there can be no monitoring, as in the invention, of the electrical variable at the control terminal of the power semiconductor device. There can be no monitoring because the control terminal voltage is not detected and because the timer 20 includes a blanking period during which, no matter what abnormality occurs, there is no monitoring and therefore no possibility of detection of an abnormality.

Moreover, the invention is superior to Kiraly in its protection of the power semiconductor device. There is no critical period of time in the invention, following the receipt of a turn-on instruction, in which the drive circuit fails to detect the electrical value at the control terminal, so that the power semiconductor device can be turned off in the event of an abnormality. During the blanking period in Kiraly, no abnormality can be detected and no action for avoiding damage to the power semiconductor device can be

undertaken. Thus, Kiraly does not provide the speed and reliability of detection of short-circuits as in the invention and, therefore, cannot even suggest the claimed invention.

For the foregoing reasons, all of the claims now pending, claims 1-7, should be allowed.

Respectfully submitted,

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